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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,163	03/28/2001	Toshiyuki Kouchi	2102475-991110	4019

26379 7590 01/29/2004

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EXAMINER	
DOOLEY, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2133	4

DATE MAILED: 01/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,163	KOUCHI ET AL.	
	Examiner	Art Unit	
	Matthew C. Dooley	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 7-10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Allowable Subject Matter

2. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record fails to teach to the limitations of claim 19 and as such, claim 19 contains allowable subject matter and would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Won et al., U.S. 6,216,240, in view of Duesman, U.S 6,169,695.

As per claim 1:

Won teaches to a plurality of DRAM circuits (Fig.1), a control circuit that receives a test control signal to perform a test control in which the RAM circuits are tested (Fig.2), an input selector that is controlled by the control circuit and inputs a DRAM macro signal to the DRAM circuitry at the time of the test (Fig.3), and an output selector that is controlled by the control circuit and outputs signals of the DRAM circuitry at the time of the test (Fig.4). However, not clearly taught by Won is the methodology of testing the DRAM circuits. Duesman teaches to testing DRAM circuitry while the access of the DRAM circuitry is changed for each row (Fig.2). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the testing methodology taught by Duesman in conjunction with the testing circuitry of Won because the implementation of the teachings of Duesman allow for reduced testing time by reducing the number of cycles required to test a memory array (Duesman: Col.1: 45-47).

As per claim 2:

The control circuit of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.1,2).

As per claim 3:

The system of Won teaches to an input selector that is controlled by the control circuit inputs a DRAM macro signal to one of the DRAM circuits during normal operation (Fig.3).

As per claim 4:

The control circuit of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.1,2).

As per claim 5:

The system of Won teaches to an output selector that is controlled by the control circuit that outputs a DRAM macro signal from one of the DRAM circuits during normal operation (Fig.4).

As per claim 6:

The control circuit of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.1,2).

As per claim 7:

Duesman teaches to accessing the first rows of the DRAM circuits while changing the access to the DRAM circuits, and following the access to the first rows, the access is performed to the next rows through the last rows of the DRAM circuits while changing the access to the DRAM circuits (Fig.2).

As per claim 8:

The control circuit of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.1,2).

As per claim 9:

Won teaches to a plurality of DRAM circuits (Fig.1), a plurality of control circuits corresponding to a RAM circuit, that receive a test control signal to perform a test control in which the RAM circuits are tested (Fig.2), and an output selector that is controlled by a

control circuit signal and outputs signals of the DRAM circuitry at the time of the test to an output terminal (Fig.4).

As per claim 10:

The control circuitry of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.1,2).

As per claim 11:

The circuitry of Won further incorporates an input terminal selector for receiving a DRAM macro signal (Fig.3).

As per claim 12:

The control circuitry of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.1,2).

As per claim 13:

The system of Won teaches to an output selector that is controlled by the control circuit that outputs a DRAM macro signal from one of the DRAM circuits during normal operation (Fig.4).

As per claim 14:

The control circuitry of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.1,2).

As per claim 15:

Duesman teaches to accessing the first rows of the DRAM circuits while changing the access to the DRAM circuits, and following the access to the first rows, the access is

performed to the next rows through the last rows of the DRAM circuits while changing the access to the DRAM circuits (Fig.2).

As per claim 16:

The control circuitry of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.1,2).

As per claim 17:

Won teaches to a plurality of DRAM circuits (Fig.1), a control circuitry that receive a test control signal and controls the DRAM circuitry simultaneously and independently (Fig.2,3), an input selector that inputs a DRAM macro signal to the DRAM circuitry at the time of the test (Fig.3), and an output selector that outputs signals of the DRAM circuitry at the time of the test to an output terminal (Fig.4).

As per claim 18:

Duesman teaches to accessing the DRAM circuits sequentially and transferring the information to outside the dram circuitry (Fig.2).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.	Morzano	U.S. 5,913,928
b.	Morgan et al.	U.S. 6,072,737
c.	Schicht	U.S. 6,163,863

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Matthew Dooley
Examiner AU 2133
01/23/04

SUPERVISORY PATENT EXAMINER